Project Report: Automated Wafer Map Defect Classification

Leveraging AI for Enhanced Semiconductor Manufacturing Insights

Table of Contents

List of Figures11. Executive Summary: The Big Picture22. Project Goal: Faster Troubleshooting, Higher Yield33. The Data: MixedWM38 Dataset Examples34. Our Approach: Building and Training the AI Classifier45. Results: Validating Model Performance56. Manufacturing Impact & Workflow Enhancement87. Recommendations & Future Work98. Conclusion9	Table of Contents	1
1. Executive Summary: The Big Picture. 2 2. Project Goal: Faster Troubleshooting, Higher Yield 3 3. The Data: MixedWM38 Dataset Examples. 3 4. Our Approach: Building and Training the AI Classifier. 4 5. Results: Validating Model Performance 5 6. Manufacturing Impact & Workflow Enhancement 8 7. Recommendations & Future Work 9 8. Conclusion. 9	List of Figures	1
 Project Goal: Faster Troubleshooting, Higher Yield	1. Executive Summary: The Big Picture	2
 The Data: MixedWM38 Dataset Examples	2. Project Goal: Faster Troubleshooting, Higher Yield	3
 4. Our Approach: Building and Training the AI Classifier	3. The Data: MixedWM38 Dataset Examples	3
 5. Results: Validating Model Performance	4. Our Approach: Building and Training the AI Classifier	4
 6. Manufacturing Impact & Workflow Enhancement	5. Results: Validating Model Performance	5
7. Recommendations & Future Work9 8. Conclusion	6. Manufacturing Impact & Workflow Enhancement	8
8. Conclusion9	7. Recommendations & Future Work	9
	8. Conclusion	9

List of Figures

Figure 1: Examples of raw input Wafer Maps from the dataset. (Source: User Provided / Manual) Figure 2: Architecture of the baseline Convolutional Neural Network (CNN). (Source: generate_model_plot.py) Figure 3: Model Training & Validation Performance Curves (Loss & AUC vs. Epochs). (Source: 2_baseline_model_training.py) Figure 4: Heatmap of Classification Metrics on Test Set (Trained Model). (Source: generate_report_heatmap.py) Figure 5: Heatmap of Simulated Poor Performance Metrics (for comparison). (Source: generate_bad_model_heatmap.py) Figure 6: Prediction Example: Test Index 15. (Source: 7_generate_report_visuals.py) Figure 7: Prediction Example: Test Index 1400. (Source: 7_generate_report_visuals.py) Figure 8: Test Set ROC Curves & AUC Scores. (Source: 3_model_evaluation.py) Figure 9: Comparison of Defect Analysis Workflow: Traditional vs. AI-Enhanced. (Source: generate_workflow_diagram.py) Figure 10: Visual summary highlighting the project's successful outcome. (Source: User Provided)

1. Executive Summary: The Big Picture

Identifying defect patterns on semiconductor wafer maps (examples shown in Figure 1) is crucial for quickly finding the root causes of production issues and improving yield. This project aimed to build an Artificial Intelligence (AI) model capable of automatically classifying various defect patterns, including complex mixed types.

What We Did: We utilized the MixedWM38 dataset, containing over 38,000 wafer maps. We developed an automated pipeline involving data loading, preprocessing, model training using a *Convolutional Neural Network* (CNN, architecture shown in Figure 2), and rigorous evaluation on unseen test data.

What Worked Extremely Well: The trained AI model demonstrated outstanding performance. It achieved very high accuracy (Overall Test AUC: 0.998, see Figure 8) in classifying defect patterns, correctly identifying most single and mixed defects (Figures 6 & 7 show specific examples). The model generalized well from the training data (Figure 3) and its per-class metrics (Figure 4) significantly outperform a hypothetical poor model (Figure 5).

Key Takeaway: AI, specifically CNNs, can be highly effective for automating the complex task of wafer map defect pattern recognition. The curated dataset proved suitable for training a robust classification model.

Manufacturing Potential: This validated model can significantly accelerate root cause analysis (Figure 9), leading to faster process corrections, improved yield, reduced waste, and optimized engineering resource allocation. The overall success is visually represented in Figure 10.

Recommendation: Proceed with deployment planning, error analysis, and exploring model explainability.

2. Project Goal: Faster Troubleshooting, Higher Yield

In semiconductor manufacturing, wafer maps visualize the pass/fail status of individual dies after electrical testing. The spatial patterns of these failures often indicate specific problems in the manufacturing process. Manual interpretation, especially for mixed defects, can be slow and subjective, hindering rapid Root Cause Analysis (RCA).

The primary goal of this project was to develop and evaluate an AI-based system to automatically and accurately classify wafer map defect patterns to accelerate RCA and ultimately improve manufacturing yield and efficiency.

3. The Data: MixedWM38 Dataset Examples

We used the publicly available MixedWM38 dataset, containing over 38,000 wafer map images (52x52 pixels) derived from electrical test data. Figure 1 provides visual examples of the typical raw wafer map data used as input to the model.

Each map is labeled according to the presence or absence of 8 basic defect types (Center, Donut, Edge_Loc, Edge_Ring, Loc, Near_Full, Scratch, Random), allowing for single and mixed-defect scenarios. The dataset originates from a real manufacturing plant and was augmented using Generative Adversarial Networks (GANs) to improve balance, although some class imbalance persists.

Data Handling Note: During initial exploration, an undocumented pixel value '3' was found. We standardized the data by clipping this value to '2' (representing a failed die) during preprocessing.



Figure 1: Examples of raw input Wafer Maps from the dataset.

4. Our Approach: Building and Training the AI Classifier

We implemented a structured machine learning workflow:

Step 1: Data Preparation (Script 1): Loaded the dataset, performed exploratory analysis, handled the data inconsistency (clipping value '3'), scaled pixel values [0, 0.5, 1.0], added necessary dimensions for the CNN, split data into Training (70%), Validation (15%), and Test (15%) sets using stratification, and saved the processed splits.

Step 2: Model Definition & Training (Script 2): A Convolutional Neural Network (CNN) was chosen. The specific architecture is depicted in Figure 2. The model was compiled using binary crossentropy loss and AUC as the key metric. Training was performed on the Training set, with performance monitored on the Validation set. Callbacks (ModelCheckpoint, EarlyStopping) ensured we saved the best performing model and prevented significant overfitting, as shown by the learning curves in Figure 3.

Step 3: Model Evaluation (Script 3 & Utilities): The best model saved during training was rigorously evaluated on the completely unseen Test set.



Figure 2: Architecture of the baseline Convolutional Neural Network (CNN).



Figure 3: Model Training & Validation Performance Curves (Loss & AUC vs. Epochs).

5. Results: Validating Model Performance

Evaluation on the unseen test data confirmed the baseline CNN model's high accuracy and reliability:

• Quantitative Metrics: The model achieved a low Test Loss of 0.0225 and an excellent overall Test AUC of 0.9980.

• Per-Class Performance: The heatmap in Figure 4 visually summarizes the detailed classification metrics (Precision, Recall, F1-Score) for each defect type on the Test set. Performance is exceptionally high (> 0.97) for almost all classes. The contrast with a simulated poorly performing model (Figure 5) starkly highlights the success achieved.





Figure 4: Heatmap of Classification Metrics on Test Set for the Trained Model.

Figure 5: Heatmap of Simulated Poor Performance Metrics (for comparison).





Figure 6: Prediction Example: Raw map vs. Model output for Test Index 15.



Wafer Map Classification - Index: 1400

Figure 7: Prediction Example: Raw map vs. Model output for Test Index 1400.



Figure 8: Test Set ROC Curves & AUC Scores.

The Story This Plot Tells:

The Goal: The ideal spot on this chart is the top-left corner (high True Positives, low False Positives). A perfect model would have a curve going straight up and then straight across, right in that corner.

Random Guessing: The dashed diagonal line represents pure random chance – a model no better than flipping a coin.

Our Model's Success: Notice how almost all the colored curves for our model are "hugging" that top-left corner. This visually demonstrates that the model is extremely good at identifying defects correctly *without* raising many false alarms. It's performing vastly better than random chance.

The AUC Score: The "AUC" (Area Under the Curve) value listed for each defect (and the averages) quantifies this performance. An AUC of 1.0 is perfect, while 0.5 is random guessing. Our model achieves AUC values very close to 1.0 (average ~0.998), confirming its excellent ability to reliably separate defective from non-defective patterns for nearly all types, even on data it hasn't seen before. This builds strong confidence in its potential for real-world manufacturing use.

6. Manufacturing Impact & Workflow Enhancement

This validated AI model offers significant practical benefits for semiconductor manufacturing by streamlining the defect analysis process, as illustrated in Figure 9. Key advantages include: Automated Classification, Accelerated RCA, Improved Yield & Reduced Waste, Enhanced Process Monitoring, Objective Data Logging, and Optimized Engineering Resources.



Figure 9: Comparison of Defect Analysis Workflow: Traditional vs. AI-Enhanced.

7. Recommendations & Future Work

The outstanding performance and clear potential impact (summarized visually in Figure 10) suggest the following next steps:

1. Deployment Planning & Integration: Prioritize developing a robust pipeline to integrate the model ('baseline_cnn_best.keras') into the manufacturing environment (MES, databases, dashboards).

2. Focused Error Analysis: Investigate the few misclassifications (especially 'Near_Full' misses) to understand edge cases.

3. Production Monitoring: Implement performance monitoring post-deployment to detect concept drift and plan for retraining.

4. Explainable AI (XAI): Employ techniques like Grad-CAM to visualize *why* the model makes specific predictions, building trust and providing deeper insights.

5. Threshold Tuning (Optional): Adjust prediction thresholds per class if specific precision/recall trade-offs are critical.



Figure 10: Visual summary highlighting the project's successful outcome.

8. Conclusion

This project successfully developed and validated a highly accurate AI model for classifying complex defect patterns on semiconductor wafer maps. The CNN demonstrated excellent generalization, proving its potential as a valuable tool to accelerate root cause analysis, enhance process control, and improve manufacturing outcomes. The path is clear for leveraging this AI capability in production.